A 12GHz-BAND SUPER LOW-NOISE AMPLIFIER USING A SELF-ALIGNED GATE MESFET

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ABSTRACT

A 12GHz-band 4-stage monolithic super low-noise amplifier has been designed and fabricated using self-aligned multi-layer gate FETs. A 0.3μm-gate FET used in the amplifier has achieved a typical noise figure of 1.07dB with an associated gain of 9.0dB at 12GHz. The amplifier gives a minimum noise figure of 1.58dB with a gain of 29dB at 12GHz and the noise figure is less than 1.76dB with an associated gain as high as 28.0dB in the frequency range from 11.7 to 12.7GHz. It is the lowest noise figure ever reported for MESFET monolithic amplifiers in the 12GHz-band.

INTRODUCTION

Recently, demands for super low-noise MMIC amplifiers have rapidly increased in microwave consumer applications such as direct broadcasting satellite (DBS) receivers. Various low-noise MMIC amplifiers have been studied by using a conventional MESFET or HEMT[1]-[4]. A low-noise HEMT MMIC amplifier with the noise figure of 1.57dB and the gain of 13.8dB at 12GHz has already been developed[1]. The conventional MESFET or HEMT reported previously has a recessed gate structure. The structure has difficulties in obtaining uniform and reproducible characteristics for lack of the controllability of the recessed depth. On the other hand, self-aligned gate planar MESFETs are superior to the conventional recessed gate FETs in uniformity and manufacturability as already demonstrated in GaAs LSI[5]. However, the self-aligned gate MESFET (SAGFET) used in GaAs digital IC is not suitable for achieving excellent noise performances of MMIC because of its higher gate resistance.

It has already been demonstrated that a new type of self-aligned multi-layer gate FET (SAMFET) with a LDD structure has lower gate resistance[6]. The SAMFET improved with a buried p-layer has been applied to a monolithic super low-noise amplifier.

In this paper, the design, the fabrication and the RF performances of the 12GHz-band monolithic low-noise amplifier using the SAMFET are described.

FET STRUCTURE AND PERFORMANCES

Figure 1 shows a schematic cross section of the SAMFET used for fabricating the low-noise MMIC. A Ti/Au layers were formed onto a WSi layer to reduce the gate resistance. The WSi layer was deposited by sputtering and etched, and then the Ti/Au layers were evaporated and lifted off to form the WSi/Ti/Au structure. The gate electrode was separated from the source/drain n^+ regions so that to reduce the gate capacitance. A lightly doped drain structure with a p-layer buried beneath an implanted channel (BP-LDD) has also been adopted to reduce gate capacitance. The layers of n,n^+,n' and p, illustrated in Fig.1, were formed in a semi-insulating LEC GaAs substrate by ion implantations of Si^+ and Mg^{++}, respectively. The ohmic electrodes were formed by AuGe/Ni/Au evaporation. Step-and-repeat lithography was used to fabricate the FET.

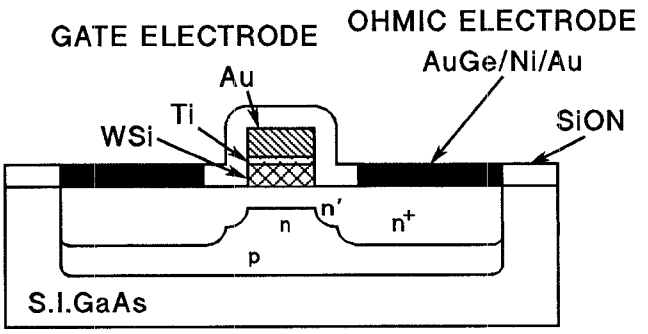

Fig. 1 Schematic cross section of the SAMFET.

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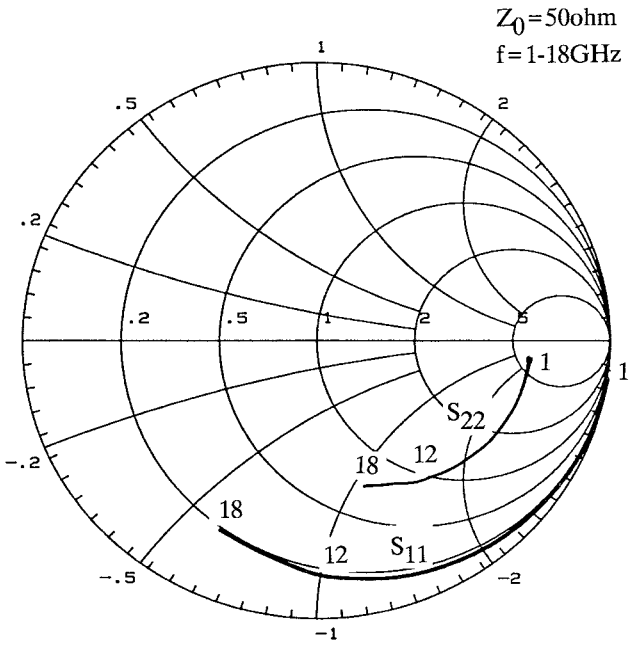
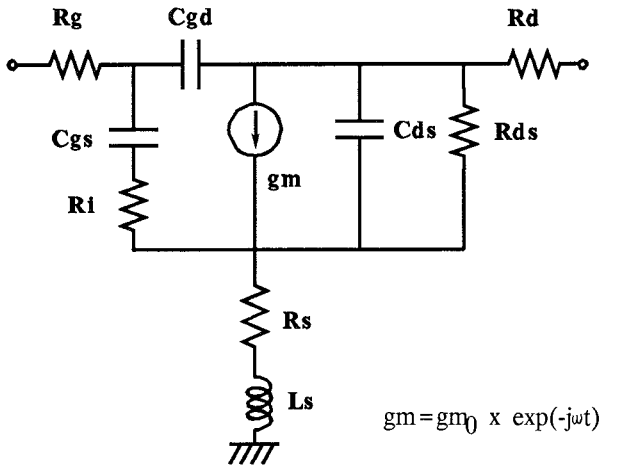


Fig. 2 S-parameter of the SAMFET.



Ls : 0.001nH Cgs: 0.145pF Cgd: 0.030pF
Cds: 0.055pF Rg : 4.37ohm Ri : 1.75ohm
Rs : 3.26ohm Rd : 10.0ohm Rds: 342ohm
gm_0: 36.0mS t : 0.75ps

Fig. 3 Equivalent circuit of the SAMFET and its element values (Wg/Lg=150μm/0.3μm).

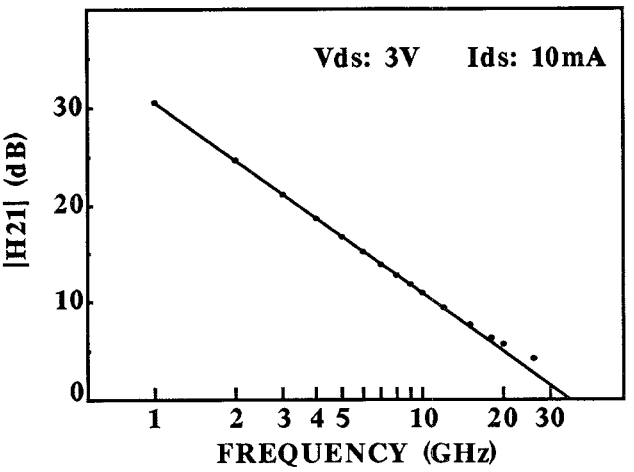
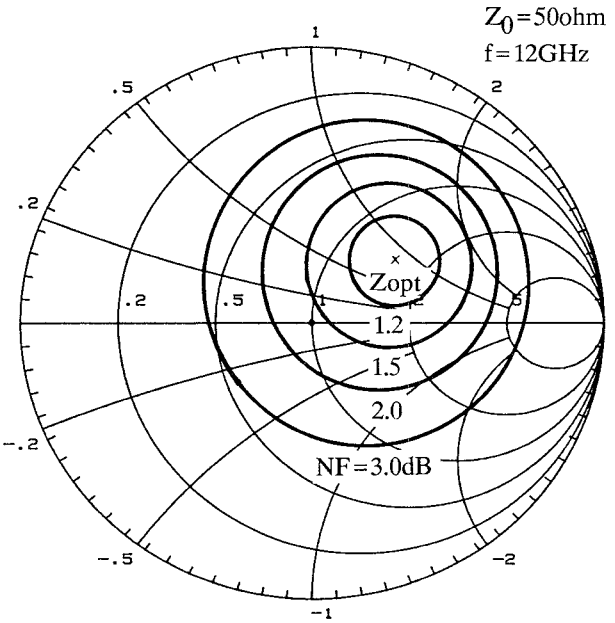


Fig. 4 Current gain (|H21|) versus frequency (Wg/Lg=150μm/0.3μm).



NFmin=1.07dB
Rn = 0.511
G_0 = 0.485
B_0 =-0.265

Fig. 5 Noise figure circles of the SAMFET. (Vds = 3 V , Ids = 10 mA)

Figure 2 shows S-parameters of the SAMFET having the total gate width of 150μm and the gate length of 0.3μm. The S-parameters were measured accurately by a on-wafer probing system. Figure 3 shows the equivalent circuit and its element values derived from the S-parameters. A typical current gain (|H21|) of the SAMFET, which was calculated from the S-parameters, is plotted in Fig.4 as a function of frequency. The cut-off frequency (f_T) is estimated to be as high as 36 GHz.

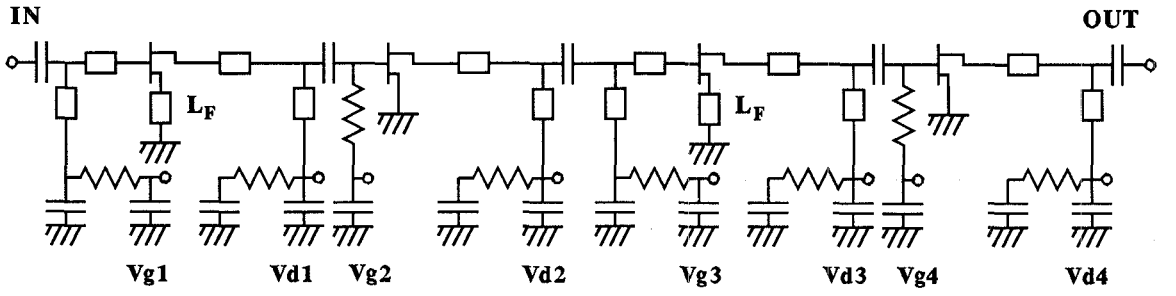


Fig. 6 Schematic diagram of the LNA.

Figure 5 shows the noise figure circles of the SAMFET. The SAMFET exhibited excellent noise characteristics: a minimum noise figure (NFmin) of 1.07dB with an associated gain of 9.0dB was obtained at 12GHz.

The amplifier includes any other components such as capacitors, microstrip lines and so on. The capacitors have the structure of metal/ insulator/metal(MIM) and with 1500Å thick SiN. The microstrip lines were formed by electroplating of 3um thick Ti/Au. The via-holes were opened at each ground of the FET and of the short stubs.

CIRCUIT DESIGN

Figure 6 shows the schematic diagram of the 12GHz-band low-noise amplifier (LNA). The amplifier has a 4-stage configuration to achieve usable gain as high as 30dB for DBS system applications. The LNA consists of four SAMFETs, an input/an output, and an inter-stage matching circuit. The matching circuits include short stubs and bias circuits. The SUPER-COMPACTsimulation program was used to optimize the matching circuits, considering a broad band operation through 11 to 13GHz. A noise figure (NF) of the amplifier mainly depends on that of the first stage. A monolithic series feedback inductor (L_F) was inserted between the source electrode for the first stage FET and the via-hole ground for getting both noise and impedance matching of an input - circuit simultaneously. However, the excess addition of the inductance (L_F) degrades the gain and the isolation of the amplifier. The value of the inductance was determined considering above merits and demerits. The value of L_F introduced at the third stage was also determined to assure a stable operation of the circuit. The inter-stage circuits were designed using conjugate matching. In each bias circuit, a stabilizing filter circuit was

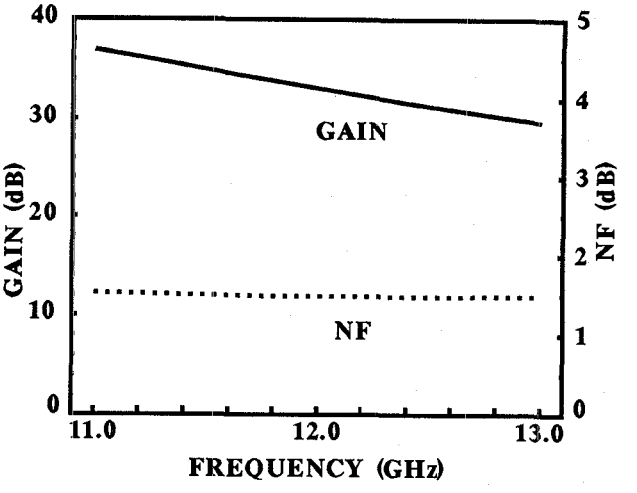


Fig. 7 Simulation results of the LNA.
(NF & Gain vs. Frequency)

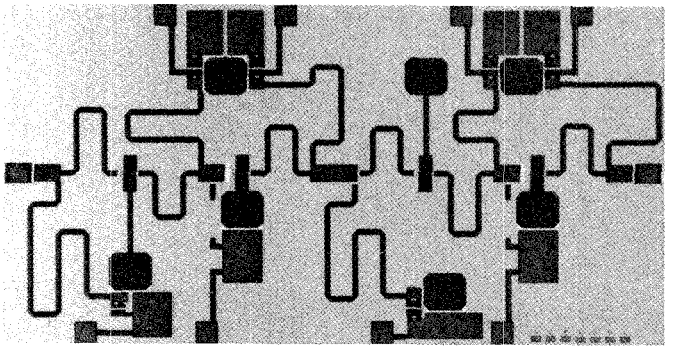


Fig. 8 Photomicrograph of the LNA
(Chip size: 3.6mm x 1.9mm).

included to prevent undesirable low frequency oscillation.

Figure 7 shows the simulation result of the amplifier. The noise figure is calculated to be less than 1.54dB with an associated gain higher than 30dB for the frequency range from 11.7 to 12.7 GHz.

PERFORMANCE

Figure 8 shows the photomicrograph of the amplifier. The total gate width and the gate length of each FET are 150μm and 0.3μm, respectively. The chip size is 3.6mm x 1.9mm, and the chip thickness is 150μm.

The frequency dependence of noise figure and the gain of the amplifier are plotted in Fig.9. The amplifier was operated at the drain bias voltage (Vds) of 3 volts and the total drain current of 40mA. Broad band operation was achieved for the frequency range from 11 to 13GHz. In the frequency range from 11.7 to 12.7GHz, the noise figure was less than 1.76dB with a linear gain higher than 28dB. These results show fairly good agreement with the simulation results. A minimum noise figure obtained in this work was 1.58dB with a gain of 29dB at 12GHz. The noise figure is the lowest ever reported for 12GHz-band MESFET monolithic amplifier fabricated on ion-implanted or epitaxial wafer. The noise performance of the SAMFET monolithic amplifier are comparable with that of the HEMT monolithic amplifier[1].

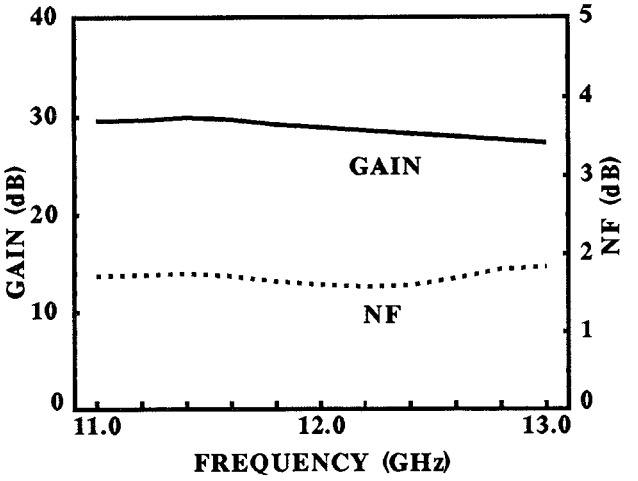


Fig. 9 Frequency dependence of the noise figure and the gain of the LNA (Vds = 3 V , Ids = 40 mA).

CONCLUSION

The 12GHz-band 4-stage monolithic super low-noise amplifier using self-aligned gate FETs has been developed. The noise figure of the LNA is less than 1.76dB with the gain higher than 28dB in the frequency range of 11.7 to 12.7GHz. These results suggest that the MMIC using the SAMFET has a promising applicability for microwave low-noise amplifications.

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